An Efficient Area Utilization of FM0, Manchester and Miller Encoding Architecture for DSRC Applications

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Abstract **—** Originally the DSRC applications requires encoding techniques for secure communication which include FM0 and Manchester encoding architecture. On analysis and observing the FM0 and Manchester encoding together in an initial hardware architecture. An effective utilization is more which leads to substantial area consumption. Hence, we adopt SOLS technique which merges architecture together and synchronize the operation. The circuit obtained is an integrated architecture of FM0, Manchester and Miller encoding to overcoming various drawbacks of traditional method. This deduced architecture of FM0 and Manchester coding would well support the DSRC standards. The performance of this paper is evaluated on Xilinx FPGA Spartan-3E kit. This paper not only develops a fully reused VLSI architecture, but also exhibits an effective performance compared with existing works.

Keywords **—** Dedicated Short Range Communication (DSRC), FM0, Manchester, Miller, Similarity Orientation Logic Simplification (SOLS), Radio Frequency Identification (RFID).

1 INTRODUCTION

FM0 and Manchester coding techniques are used to encode the data while transmit the signal through medium. Using similarities in the FM0 and Manchester coding, we developed the reused VLSI hardware architecture.

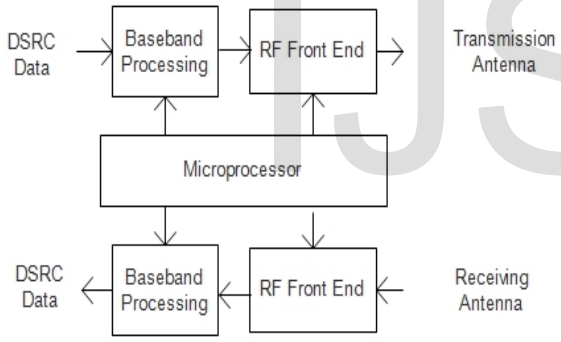

Figure 1. DDFS system architecture.

Since, encoding plays the vital role in secured communication. Developing architecture for such encoding techniques is need of the hour. One sort of renowned and commonly used communication technique is DSRC (Dedicated Short Range Communication) which is designed support the variety of applications (Figure 1). Based on vehicular environments communication. DSRC, the subset of RFID (Radio Frequency Identification) for tracking and identification. DSRC standards adopts both FM0 and Manchester encoding for signal reliability and dc balance.

2 CODING PRINCIPLES OF FM0, MANCHESTER AND MILLER ENCODING

The coding principles of FM0 and Manchester encoder are discussed as follows,

2.1 FM0 encoding

FM0 encoding is also called as bi-phase space encoding scheme. In FM0 encoding, the signal to be transmitted and done according (Figure 2), to the following rules,

- It inverts the phase of the base band signal at the boundary of each symbol.
- For representing logic '0' level, it inverts the signal at the mid of the symbol.
- For representing logic '1' level, it constant voltage occupying an entire bit window.

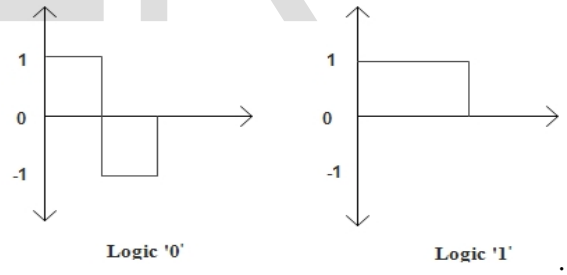

Figure 2. FM0 basis Functions

2.2 Manchester Encoding

Manchester code be first developed by G.E.Thomas at 1949. It is also called as phase encoding scheme. In Manchester encoding, the signal to be transmitted and done according (Figure 3) to the following rules,

- A '1' is noted, when low to high transition occurs.
- A '0' is noted, when high to low transition occurs.

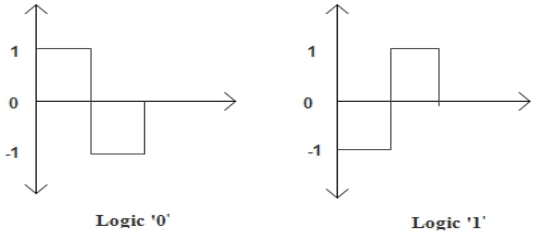

Figure 3. Manchester basis Functions

2.3 Miller Encoding

Miller encoding is also known as delay encoding. It can be used for higher operating frequency and is similar to Manchester encoding except that the transition occurs in the middle of an interval when the bit is 1. While using the Miller delay, noise interference can be reduced. In Manchester encoding, the signal to be transmitted and done according (Figure 4) to the following rules,

- Phase inversion occurs at data '1' symbol.
- Phase changes when the logic '1' data appears after the long continuous logic '0' data.

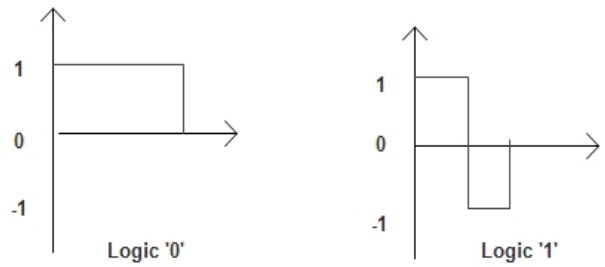

Figure 4. Miller basis Functions

3 INITIAL HARDWARE ARCHITECTURE OF FM0 AND MANCHESTER ENCODING

The hardware architecture of Manchester encoding is as simple as XOR operation. However, the hardware architecture for FM0 is not as simple as that of Manchester Initial hardware architecture of FM0 and Manchester encoder is shown in the (Figure 5). The top part is the hardware architecture of FM0 encoder and the bottom part is hardware architecture of Manchester encoder. The Q_a and Q_b store the state code of the FM0 code. The Mux_1 is to switch Q_a and Q_b through selection of clock (CLK) signal. The determination of which coding is adopted depends on the mode selection of Mx_2, where the mode=0 is for FM0 code and mode=1 is for Manchester code.

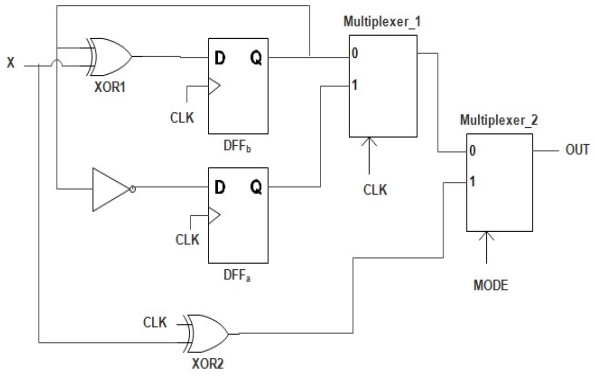

Figure 5. Initial Hardware architecture of FM0 and Manchester encodings

The transient equation of FM0 and Manchester encoding is,

- FM0 Encoding equation is

$$T1 = CLK_{bar}.Q_a + CLK.Q_b \quad (1)$$

- Manchester Encoding equation is

$$T2 = X \oplus CLK = X.CLK_{bar} + X_{bar}.CLK \quad (2)$$

The Finite State Machine (FSM) of FM0 encoding has classified into four states are S0, S1, S2 and S3. The FSM of FM0 has conduct the state diagram of each state, as shown in (Figure 6). From the state diagram, transition table to be formed, as shown in Table 1.

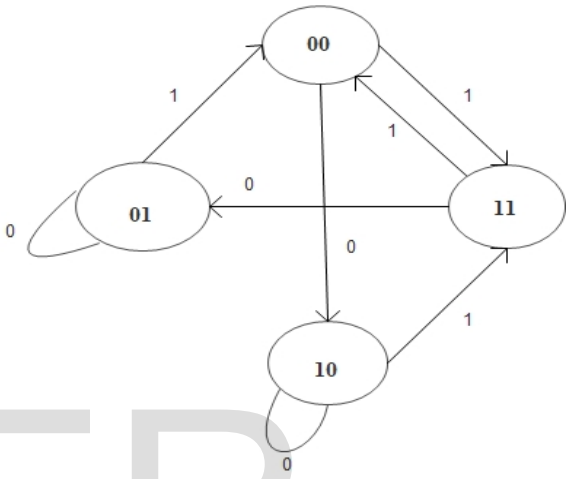

Figure 6. FSM of FM0 State diagram

The initial hardware architecture (Figure 5) consumes more area as it involves separate architectures for FM0 and Manchester encoding operations mode '0' and mode '1' respectively. This is turn cause large energy consumption and where in both the operation is carried out in a single architecture namely the SOLS (Similarity Orientation Logic Simplification) architecture.

Table I
Transition table

Present State		Next State			
		Q_a^+		Q_b^+	
Q_a	Q_b	X=0	X=1	X=0	X=1
0	0	1	1	0	1
0	1	0	0	1	0
1	1	0	0	1	0
1	0	1	1	0	1

4 SIMILARITY ORIENTATION LOGIC

SIMPLIFICATION OF FM0 AND MANCHESTER ENCODING ARCHITECTURE

The purpose of SOLS (Similarity Orientation Logic Simplification) technique is classified into two core techniques. They are namely area compact retiming and balance logic-operation sharing (BLOS). Finally, the performance evaluation of the SOLS technique is given.

4.1 Area Compact Retiming

The logic for Q_a and the logic for Q_b are the Boolean functions. For FM0, the state code of each state is stored into DFF_A and DFF_B. The transition of state code only depends on instead of both Q_a^+ and Q_b^+. Thus, the FM0 encoding just requires a single 1-bit flip-flop to store the Q_b^+. If the DFF*A* is directly removed, a non-synchronization between Q_a and Q_b causes the logic fault of FM0 code. To avoid this logic-fault, the DFF_B (Figure 7) is relocated right after the MUX−1.

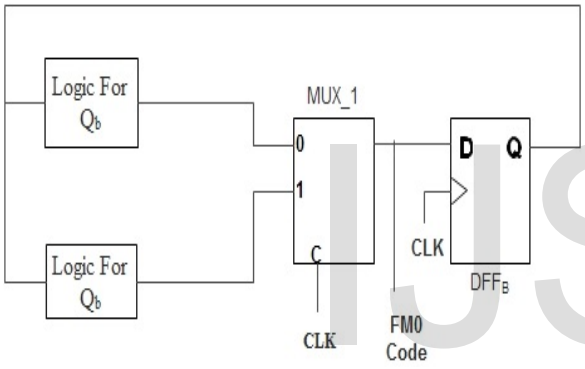

Figure 7. FM0 encoding with area compact retiming

4.2 Balance Logic Operation Sharing

The FM0 and Manchester logics have a common point of the multiplexer like logic with the selection of CLK. The concept of balance logic operation sharing has integrate with the X_{bar} into Q_a and X into Q_b, respectively. The Q_a can be derived from an inverter of Q_b^+, and *X* is obtained by an inverter of *X*. The logic for Q_a/X can share the same inverter, and then a multiplexer is placed before the inverter to switch the operands of Q_b^+ and *X*. The Mode indicates either FM0 or Manchester encoding is adopted.

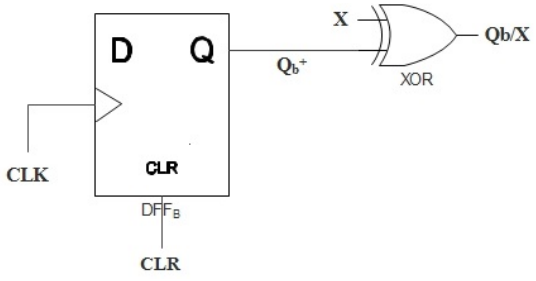

Figure 8. Balance logic operation sharing of DFF_B

The clear (CLR) signal is used to reset the content of DFF*B* to logic '0'. The DFF*B* (Figure 9) can be set to zero by activating CLR for Manchester encoding. When the FM0 code is adopted, the CLR is disabled, and the Q_b^+ can be derived from DFF*B*. The proposed architecture using SOLS technique to integrate both FM0 and Manchester architectures. The XOR function (Figure 9) produce glitch and causing logic fault on coding. The XOR in the logic for Q_b/X is translated into the XNOR with an inverter, and then this inverter is shared with that of the logic for Q_a/X_{bar}.

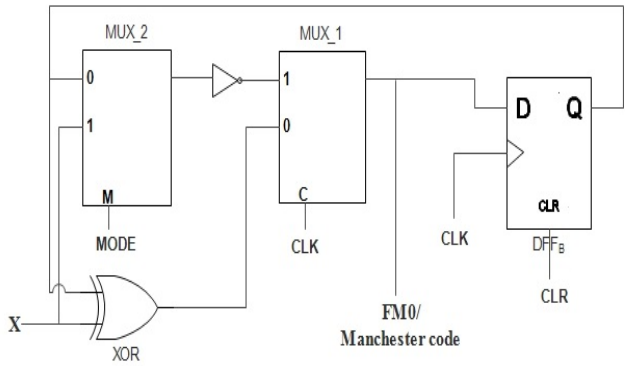

Figure 9. XOR operation between Q_a/X_{bar} and Q_b/X

If the CLR is simply derived by inverting Mode without assigning an individual CLR control signal, this leads to a conflict between the coding mode selection and the hardware initialization. To avoid this conflict, both Mode and CLR are assumed to be separately (Figure 10) allocated to this design from a system architecture. Therefore, FM0 and Manchester encoding is adopted and no logic component of the architecture is wasted. Every component is active in both FM0 and Manchester encodings.

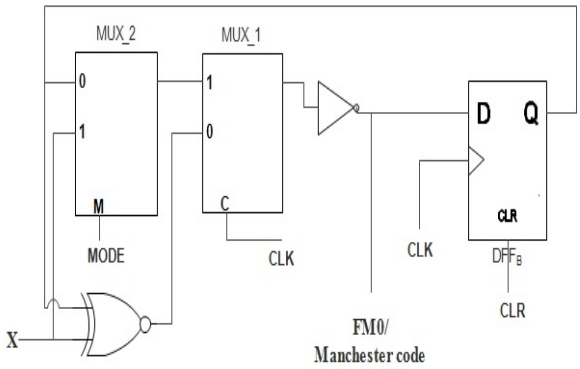

Figure 10. XNOR operation between Q_a/X_{bar} and Q_b/X

5 EXPERIMENT RESULTS

FM0 Encoding and Manchester Encoding are be simulated by using Xilinx software through Verilog HDL coding . Depending upon the data value output to be changed through selecting Reset, CLR and MODE The initial hardware architecture does not have CLR function and have only MODE function to select

FM0 or Manchester operation (Figure 12(a) and 12(b)). The schematic view of initial hardware architecture

is shown in Figure 11. But, SOLS technique has integrate both FM0 and Manchester code and it can be selected by clear (CLR) and MODE signals (Figure 14(a) and 14(b)).

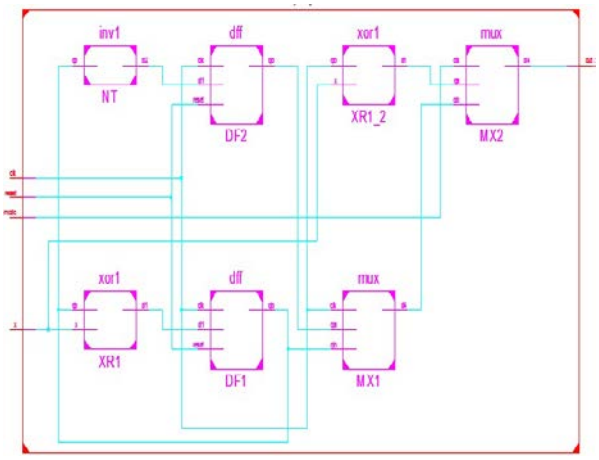

Figure 11. Schematic diagram of an initial hardware architecture of FM0 and Manchester encoding

The schematic diagram of SOLS technique is shown in Figure 13. By using CLR signal, we avoid conflict and logic fault and similarly using MODE signal to select FM0 or Manchester operation. If CLR signal is '0' and MODE signal be '1', then it select Manchester code. Similarly, if CLR signal is '1' and MODE signal be '0', then it select FM0 code. Depending up on the data value, output bit changes per clock cycle.

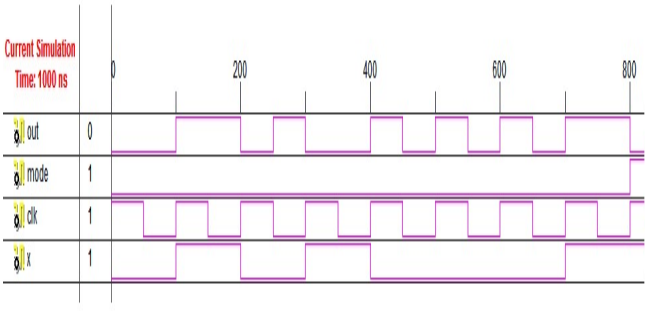

Figure 12(a). Simulation result of initial hardware architecture of FM0 encoding

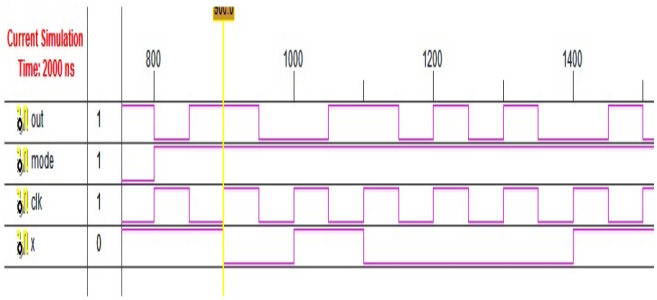

Figure 12(b). Simulation result of initial hardware architecture of Manchester encoding

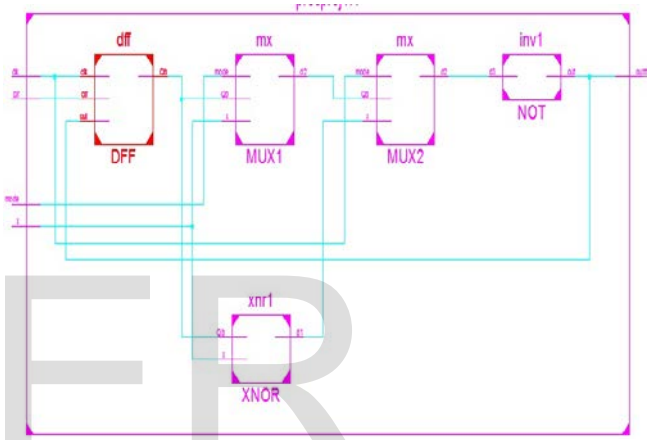

Figure 13. Schematic diagram of FM0 and Manchester encoding using SOLS technique

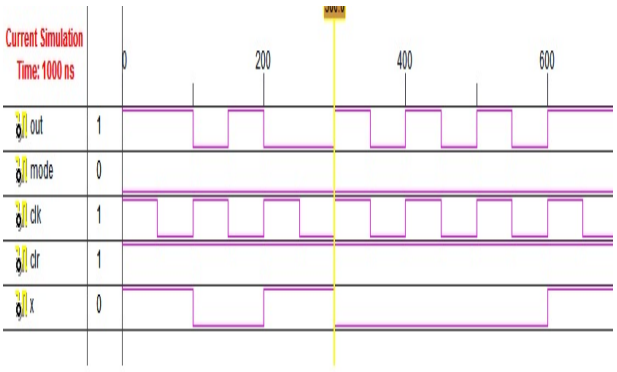

Figure 14(a). Simulation result of FM0 encoding using SOLS technique

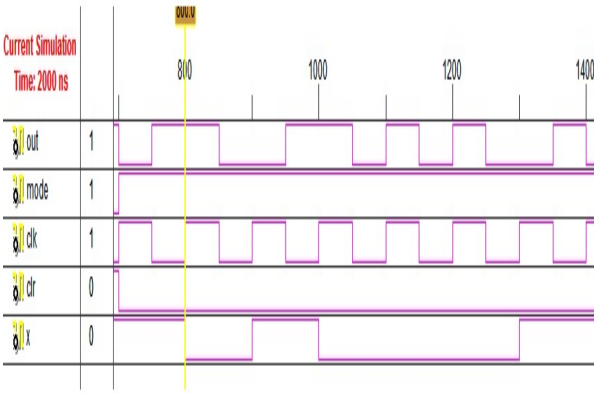

Figure 14(b). Simulation result of Manchester encoding using SOLS technique

Using the Xilinx ISE 9.2i, I calculated the below data's by Xilinx Xpower Analyzer tool. I compare Area and Power for both initial hardware of FM0 and Manchester encoding architecture and for SOLS technique architecture of FM0 and Manchester code as shown in table II.

Table II
Comparison

Terms	Initial Hardware Architecture	SOLS Technique Architecture
Number of Slices	3	1
Number of Slices Flip Flops	2	1
Number of 4 input LUTs	5	2
Number of IOs	5	5
Number of bonded IOBs	5	5
Number of Clocks	1	1
Leakage Power	52.3mw	52mw
Quiescent Power	52.3mw	52mw

6 CONCLUSION AND FUTURE VIEW

6.1 Conclusion

Using similarities in the FM0 encoding and Manchester encoding techniques, hardware architecture is to be developed. Manchester and FM0 coding are very popular codes, as these codes are level insensitive, self-clocking and they provide signal absence detection and having the encoding clock rate embedded within the transmitted data. They encode the data as 1's and 0's. FM0 and Manchester encoding architectures combined together to form efficient compact architecture through SOLS (Similarity Orientation Logic Simplification) Technique. The SOLS technique is done on hardware utilization by means of two core techniques. They are namely area compact retiming and balance logic operation sharing (BLOS). FM0 coding and Manchester coding equations are combined in balance logic operation sharing. This deduced architecture of FM0 and Manchester coding would well support the DSRC standards.

6.2 Future View

Now, we plan to start the development and analysis of Miller encoding integrate with FM0 and Manchester encoding architecture for the application of Dedicated Short Range Communication (DSRC). These three encodings have same similarities and clock rate embedded within the transmitted data. Using similarities in the FM0, Manchester and Miller techniques, hardware architecture is to be develop using SOLS technique.

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